ABSTRACT

A reduced instruction set computer architecture implemented on a field programmable gate array includes a parallel bit shifter capable of reversible shifts and bit reversals, a Reed-Muller Boolean unit coupled to the parallel bit shifter and an immediate instruction function using a half-word literal field in an instruction word that impacts a whole word logically through a combination of modes that variously manipulates the distribution of a set of literal bits of the half-word literal field across the instruction word.